VBG08H-E

Ignition coil driver power I.C.

Datasheet - production data

OctaPAK 7+1

Features

HV_{CL}	I_{NOM}	V_S	I_S
360 V	8 A(1)	6 - 40 V	5 mA

1. Max operative current

- Smart electronic ignition with embedded IGBT power stage
- Coil current limiter
- Current threshold flag diagnostic output
- Enable pin
- Slow turn-on
- Soft shut down (SSD) operated by low voltage clamp circuit (LVC)
- SSD activated by
  - Thermal intervention (T_j > 150°C)
  - Enable pin
  - Input overvoltage
  - Battery overvoltage
- Battery fault tolerant pins
- ESD protected
- TTL compatible

Description

VBG08H is a single channel driver, plus an IGBT power stage internally assembled using Chip On Chip (COC) hybrid technology.

The two chips are assembled together in the OctaPAK® package.

The device comes with several built-in protections like a coil current limiter, thermal monitoring circuit, which triggers a Soft Shut Down (SSD) as soon as the maximum allowable temperature is reached (TSD). It avoids extra voltage on the secondary side of the coil transformer.

The Slow Turn On circuit (STO), avoids unwanted sparks during first negative dV/dt of HVC voltage at turn on.

The current flag circuit provides an output logical signal voltage when the coil current reaches a fixed threshold.

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
OctaPAK	VBG08H-E	VBG08HTR-E

This is information on a product in full production. www.st.com

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1 Detailed description

VBG08H is a single channel driver, plus an IGBT power stage internally assembled using Chip On Chip (COC) hybrid technology. The Power Stage integrates the current shunt resistor for sensing the coil current, and the thermal diode for monitoring the temperature which triggers the TSD intervention.

The two chips are assembled together in the OctaPAK® package. The device is intended for driving huge inductive loads in harsh automotive environments (as electronic ignitions). The functional block diagram is shown in *Figure 1*.

The IGBT is controlled by the input signals pin INP. In particular, when the device is enabled (EN pin is at “0”), the transition low to high of INP pin turns-on the IGBT, while, the transition high to low of the same input signal, turns-off the IGBT causing an extra voltage on the secondary side of the coil transformer, generating a spark in the spark system plug.

The implemented features offer a specific design advantage that makes the VBG08H particularly suitable for E.C.U. applications.

The device comes with several built-in protections like a coil current limiter, a thermal monitoring circuit, which triggers a Soft Shut Down (SSD) as soon as the maximum allowable temperature is reached (TSD), avoiding to generate an extra voltage on the secondary side of the coil transformer.

Soft shut down is performed using a Low Voltage Clamp (LVC) circuit, which clamps the primary coil winding at a fixed voltage, with respect to the battery value: LVC is activated as the result of a logical OR combination among different fault conditions: thermal shutdown, input overvoltage, internal wire bonding disconnection, supply overvoltage, device disabling in ON-state (EN pin pulled high while INP pin is high).

All these fault events trigger the soft shut down operation and cause a slow discharge of the coil current, avoiding generating any undesired sparks.

If SSD is activated by TSD, the complete slow coil current discharge depends on the duration of input signal in the high state. If the input signal is high for a time longer than the coil discharge time, the SSD stays activated until the coil is completely discharged (zero coil current).

Anyway, if the input command signal arrives while the SSD is active, the LVC is immediately disabled for allowing the spark generation with the residual energy.

SSD timing diagrams are shown in *Figure 7*, *Figure 8* and *Figure 9*.

In case of thermal intervention, the IGBT remains switched off until the internal junction temperature, decreasing, reaches a lower temperature threshold, which corresponds to the fixed temperature hysteresis. In addition to the built-in protections above described, the chip is equipped with a single current flag diagnostic output.

Current Flag circuit provides an output logical signal voltage, which goes low (after a filtering time) when the input control pin goes high, and returns high when the coil current reaches a fixed value threshold. An internal voltage regulator, connected to the battery pin V_S supplies all the internal circuitry.

The EN pin is intended as chip enable pin and it is used for enabling / disabling the device (see *Figure 6*).

The event “EN pulled high” is stored inside internal register and causes the complete slow discharge of coil current.

Device can restart when the EN pin is pulled low and after the first low to high transition of the input pin. *Figure 12*, *Figure 13*, *Figure 14* and *Figure 15*, show device behavior, with different combinations of INP and EN signal pins. This pin is provided with an internal pull-up current source, which disables the chip by default, in case the pin is left floating.

1.1 Slow turn-on

Device is internally equipped with a completely integrated Slow Turn On circuit (STO), that helps avoiding unwanted sparks during first negative dV/dt of HVC voltage at turn on (see *Figure 5*).

1.2 Input over voltage (INP_OV)

Device is internally equipped with a built in protection which is activated in case of command input pin over voltage. If the input pin is shorted with a supply voltage (V_{BATT} or V_S), which is above the internal fixed threshold “$INP_{_OV_TH_H}$”, the device operates a soft shutdown which slowly discharges the coil current. This event is managed by the device as a “real time event”, so the completion of coil current discharge depends on the time duration of the INP_OV detection. As soon as the INP_OV condition is removed (voltage at input pin decreases below the second lower threshold voltage “$INP_{_OV_TH_H}$ - $INP_{_OV_HYS}$”), the device can be switched on, if a normal high state voltage is applied on the command input pin. See *Figure 16* for more details.

1.3 Battery overvoltage

When the supply voltage V_S overcomes the "$V_{S_OFF_TH}$" (battery load dump) for a time longer than 220 µs (typ), the device operates a soft shutdown until the complete coil current discharge. The device remains switched off until the battery voltage falls under the second lower threshold voltage, which corresponds to the prefixed hysteresis parameter “$V_{S_OFF_HYS}$”.

Once this condition is verified, only a low to high transition of command input pin can turn on the device. See *Figure 17* for more details.

2 Block diagram

Figure 1. Block diagram schematic

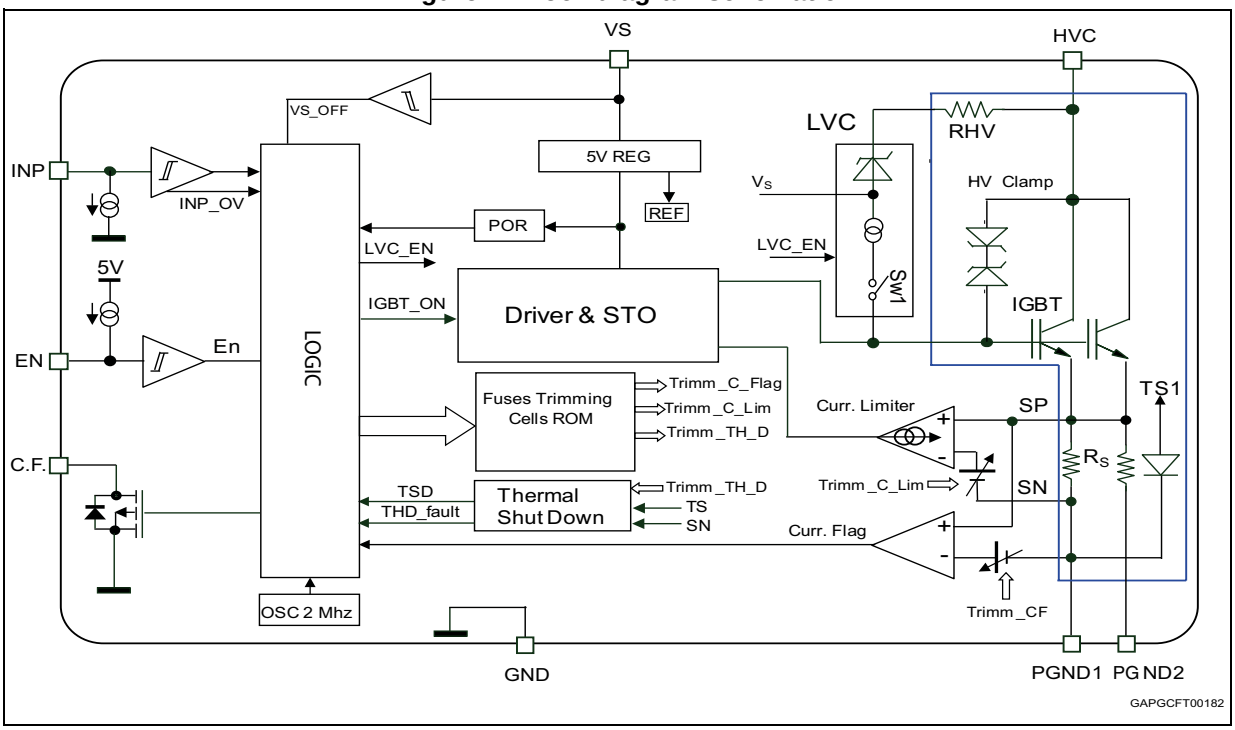


Figure 2. OctaPAK top view

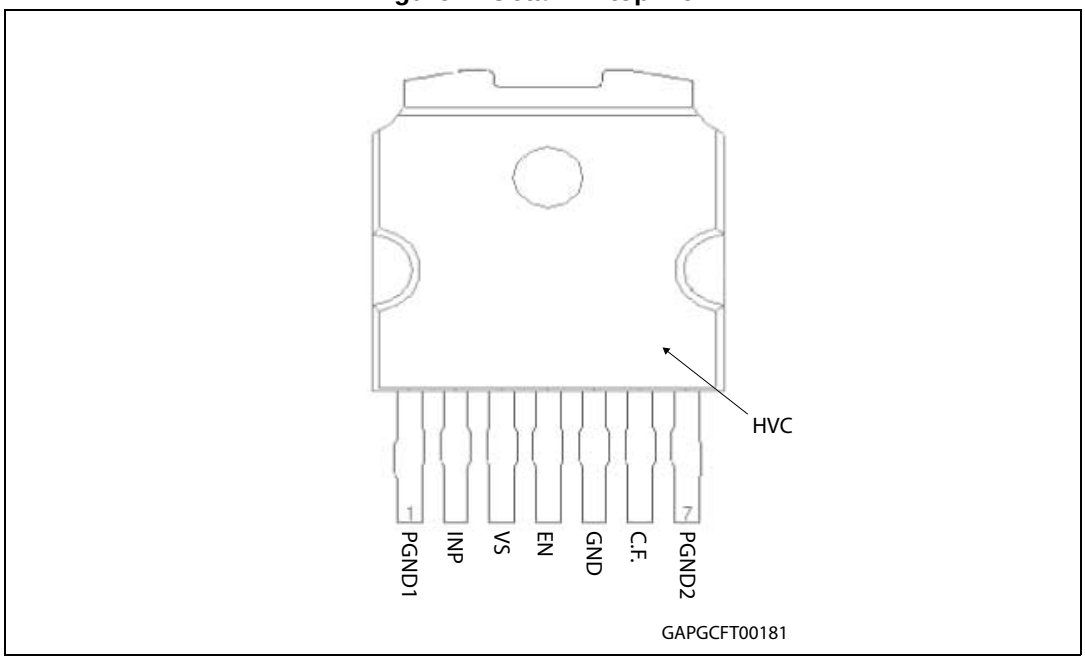


Table 2. Pin name and function

Pin number	Pin name	Pin function
1	PGND1	Power GND
2	INP	Input control pin / pulled down if left floating
3	V_S	Battery supply voltage
4	EN	Chip enable control pin / pulled up if left floating
5	GND	Controller GND
6	C.F.	Current flag output / open drain
7	PGND2	Power GND
TAB	HVC	IGBT HV collector

3 Electrical specifications

Figure 3. Voltage and current conventions

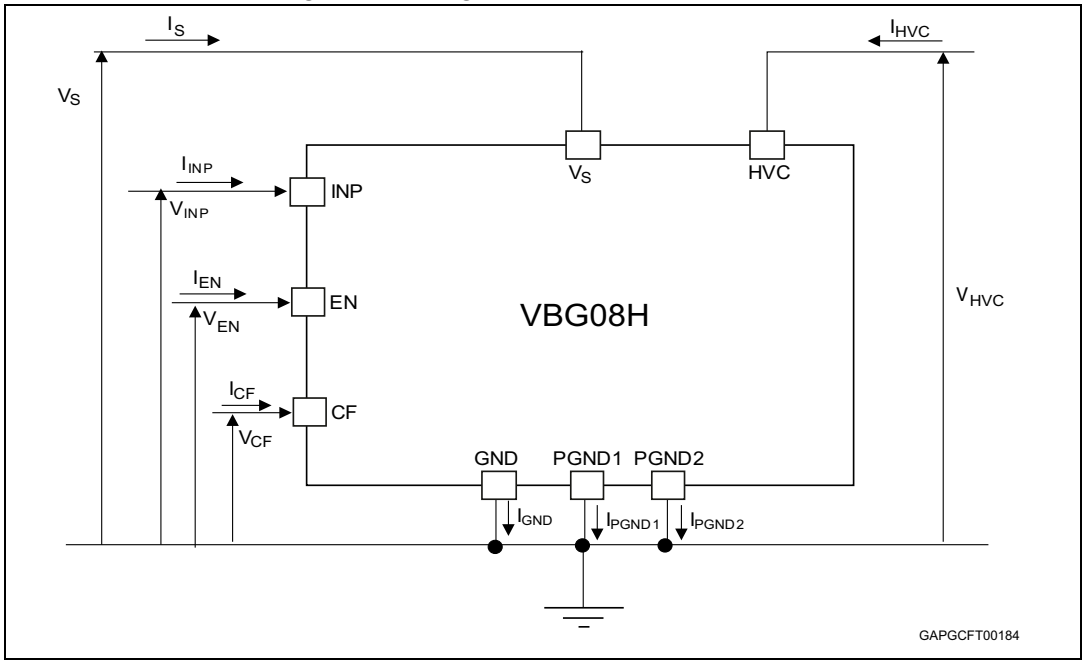


Figure 4. Application circuit

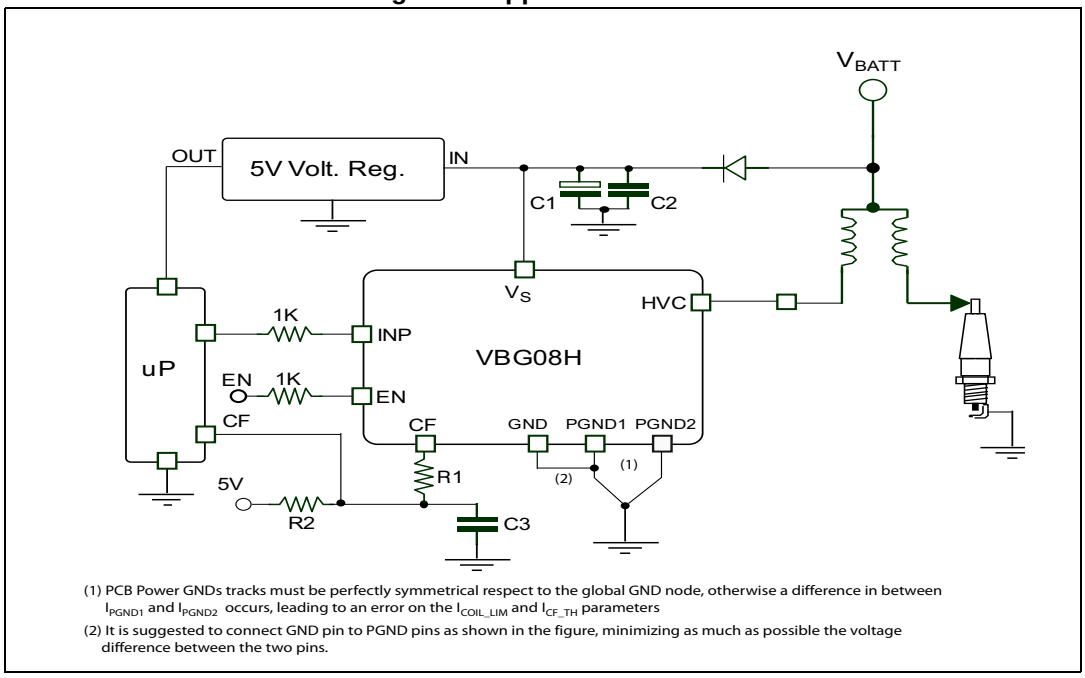


Table 3. Suggested component values for the application circuit

Type	Description	Value
R1	C_{Flag} filter resistor	1 K
R2	C_{Flag} filter resistor	≥ 4 K
C1	V_{CC} capacitor	100 nF
C2	V_{CC} capacitor	10 µF
C3	C_{Flag} filter capacitor	(1)

1. Application dependent.

3.1 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 4* may cause permanent damage to the device itself. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 4. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_{HVC}	Collector voltage (internally limited)	-16 to V_{clamp}	V
I_{HVC}	Collector current (internally limited)	Internally limited	A
V_S	I.C. supply voltage range	-0.3 to 40	V
V_{INP}	Input voltage	-0.3 to 28	V
V_{CF}	Current flag output voltage	-0.3 to 5.5	V
I_{CF}	Flag output current	1.5	mA
V_{EN}	Enable voltage	-0.3 to 28	V
ESCIS25	Single pulse SCIS energy (T_j = 25°C; L = 6 mH)	265	mJ
ESCIS150	Single pulse SCIS energy (T_j = 150°C; L = 6 mH)	175(2)	mJ
V_{ESD}	ESD voltage (HVC pin) (HBM: R = 1.5 KΩ; C = 100 pF)	4	KV
V_{ESD}	ESD voltage (all pins) (HBM: R = 1.5 KΩ; C = 100 pF)	2	KV
T_j	Operating junction temperature	-40 to 175	°C
T_{stg}	Storage temperature range	-55 to 175	°C
$I_{(HVC)_UNDGND}$	Max underground collector current (t_app ≤ 100 µs)	-6	A
t_{SC_MAX}	Short circuit withstand time R_{SC} = 0 Ω; I_{HVC} = 10.5 A (maximum current limitation) – V_S up to 16 V – 16 V < V_S ≤ 24 V – 24 < V_S ≤ 28V	 No constrains 5 2	 ms ms

1. Refer to *Figure 3* for voltage or currents conventions.
2. In case of the device switch-off occurs in current limitation with open secondary condition, the energy limit must not be exceeded. The double fault condition is not provided.

3.2 Thermal data

Table 5. Thermal data (estimated)

Symbol	Parameter	Value	Unit
$R_{tj\text{-}case}$	Thermal resistance junction-case	0.55	°C/W
$R_{tj\text{-}amb}$	Thermal resistance junction-ambient	see *Figure 24*	°C/W

3.3 Electrical characteristics

-40°C < T_j < 150°C; V_S = 6 ÷ 28 V, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{HV_CLAMP}	V_{HVC} high voltage clamp	I_{HVC} = 6.5 A	320	360	400	V
V_{LV_CLAMP}	V_{HVC} low voltage clamp	I_{HVC} = 6.5 A	V_S + 7	V_S + 10	V_S + 13	V
V_{CE_SAT1}	V_{HVC}: collector to emitter saturation voltage	V_S = 13.5 V; I_{HVC} = 4 A			1.5	V
V_{CE_SAT2}	V_{HVC}: collector to emitter saturation voltage	V_S = 13.5 V; I_{HVC} = 6.5 A			1.8	V
I_{S_STBY}	Standby supply current	IN = 0; EN = 0; IN = X; EN = 1; V_S = 13.5 V		5	6	mA
V_S	Operative DC supply voltage		5.4		28	V
$V_{S_OFF_TH}$	V_S overvoltage threshold		29	32	35	V
$V_{S_OFF_HYS}$	V_S overvoltage hysteresis		0.5		3	V
I_{COIL_NOM}	Operative coil current range		0		8	A
I_{COIL_LIM}	Coil current limit	-40°C < T_j < 125°C; V_S = 6 V			10.5	A
		-40°C < T_j < 125°C; 9 V ≤ V_S ≤ 28 V	8.5	9.5	10.5	A
I_{CES}	Collector current (including the RHV contribution)	V_{CE} = 28 V; V_{INP} = 0 V; T_j = 125°C	0.3		1	mA
V_{INP_H}	High level input voltage		3			V
V_{INP_L}	Low level input voltage				1.5	V
V_{INP_HYS}	Input threshold hysteresis		0.2			V
I_{IN_PDW}	Input pull down current	V_{INP} = 4 V	10	20	30	µA
$INP_{_OV_TH_H}$	Input overvoltage activation threshold		8	9	10	V

Table 6. Power section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$INP_{_OV_HYS}$	Input overvoltage hysteresis		0.8	1.4	2	V
V_{CF_L}	Low level C.F. output voltage	I_{CF} = 1 mA			0.8	V
$I_{CF_leakage}$	Leakage current on flag output	V_{INP} = 0; V_{CF} = 4 V; V_S = 13.5 V			10	µA
$I_{CF_TH_6.5}$	Coil current level threshold 6.5 A(1)	-40°C ≤ T_j < 25°C	5.85		7	A
		25°C ≤ T_j < 100°C	6		6.85	
		100°C ≤ T_j < 125°C	6.2		6.8	
		125°C ≤ T_j ≤ 150°C	6.05		6.95	
T_{SSD}	Thermal shutdown intervention		150		175	°C
T_{SSD_HYS}	Thermal hysteresis		17	25	33	°C
V_{EN_H}	High level enable voltage		3			V
V_{EN_L}	Low level enable voltage	V_{OUT} free to follow V_{INP}			1.5	V
V_{EN_HYS}	EN input hysteresis		0.2			V
$-I_{EN_PU}$	Enable pin pull up current	V_{EN} = 0 V	10	20	30	µA

1. See *Figure 18: Current flag threshold vs temperature for I_{FLAG} = 6.5 A*).

Table 7. Timing characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK}			1.5	2	2.5	MHz
t_{FT_CF}	Current flag filtering time			$16/f_{CLK}$		µs
t_{FT_EN}	Enable filtering time			$32/f_{CLK}$		µs
t_{FT_INP}	Input filtering time			$32/f_{CLK}$		µs
td_{ON}	Delay time from INP rising edge to V_{HVC} = 0.9 V_S (see *Figure 5*)	EN = 0; T_j = 25°C			30(1)	µs
$(\Delta V_{HVC}/\Delta t)_{ON}$	HVC slope during turn-on (see *Figure 5*)	EN = 0; T_j = 25°C; V_S = 13.5 V	0.1	0.3	1	V/µs
td_{OFF}	Delay time from INP falling edge to V_{HVC} = 100 V (see *Figure 5*)	EN = 0; T_j = 25°C			15	µs
HVC_{3V}	STO deactivation threshold	T_j = 25°C; V_S = 13.5 V		3	5	V

1. Including t_{FT_INP}.

Figure 5. Input control vs V_{HVC} time definitions

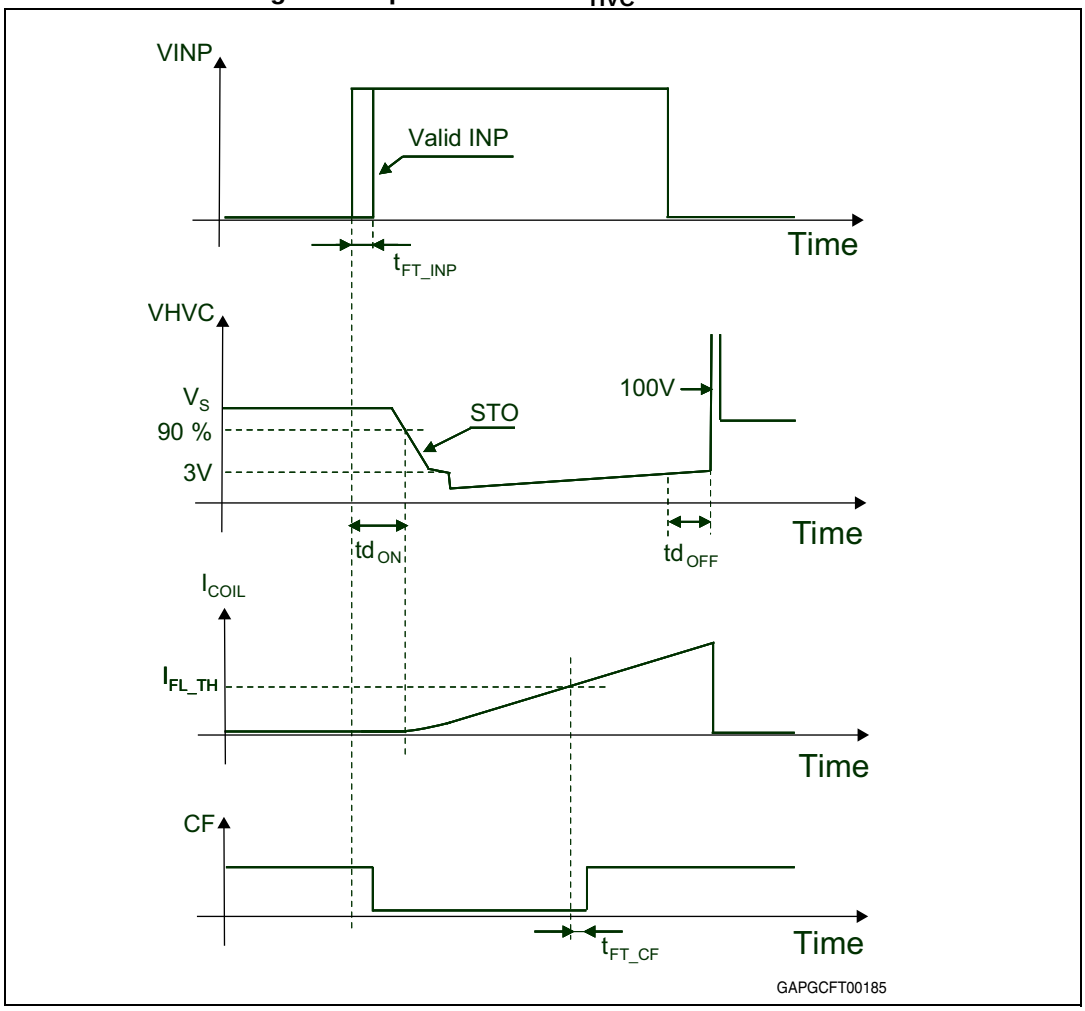


Figure 6. Electrical characteristics timing

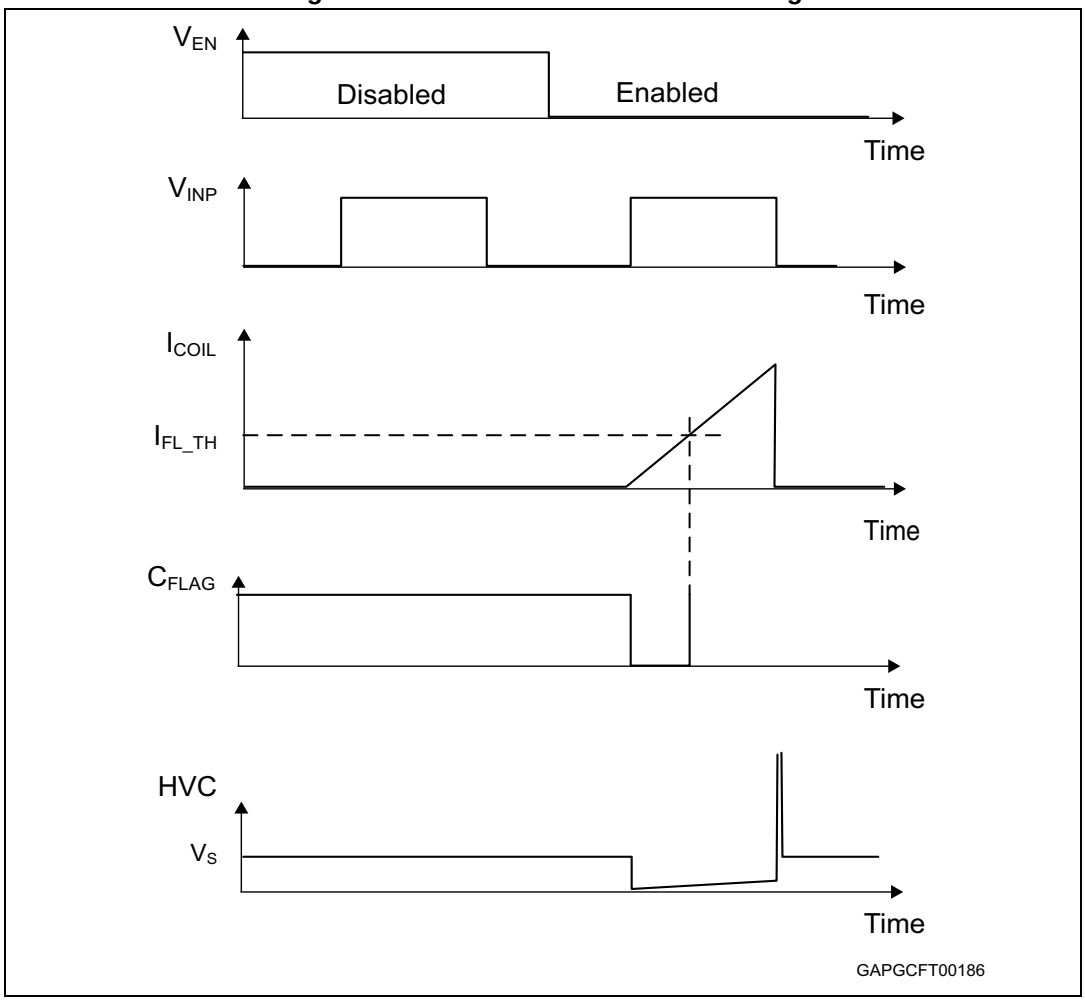


Figure 7. Current limit without TSD activation T_j < TSD

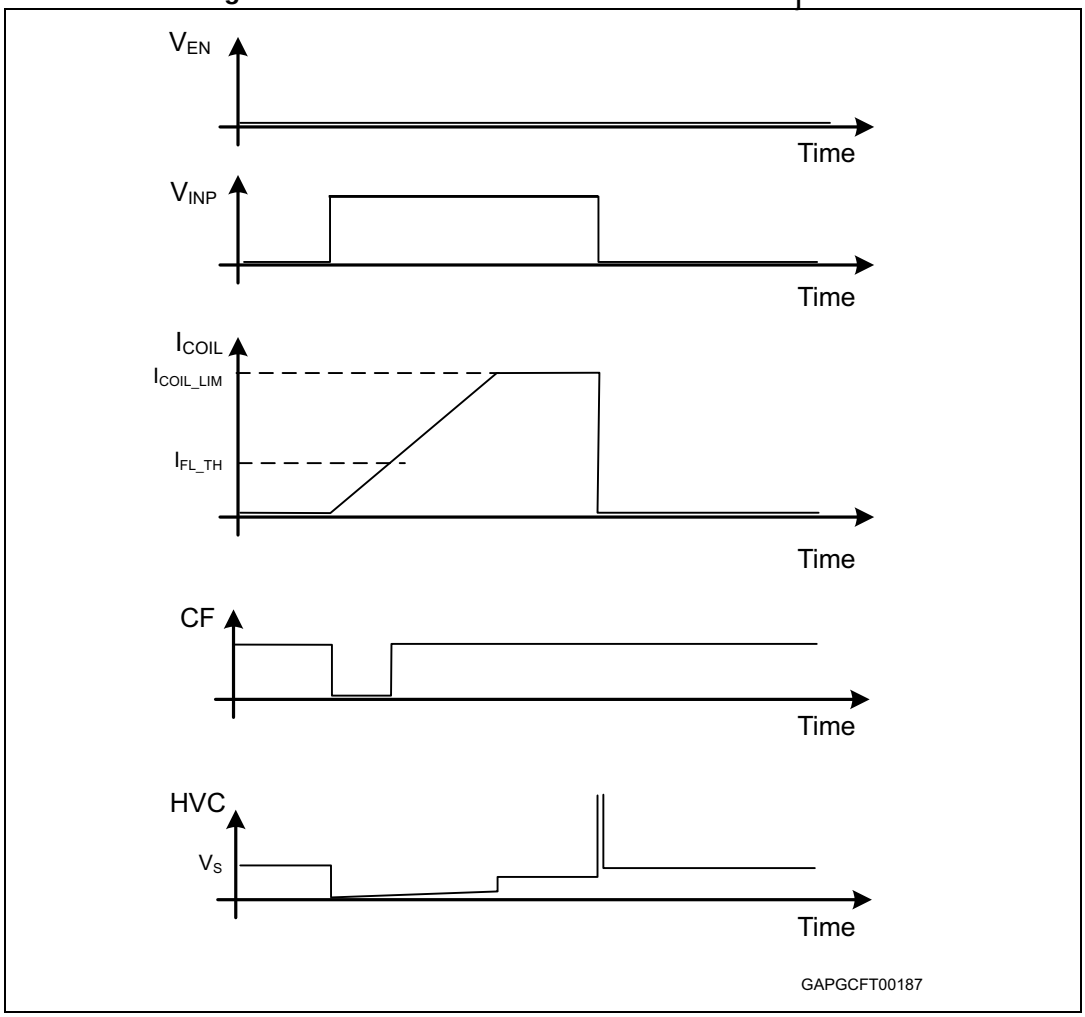


Figure 8. Current limit followed by TSD activation (T_j = TSD) (case 1)

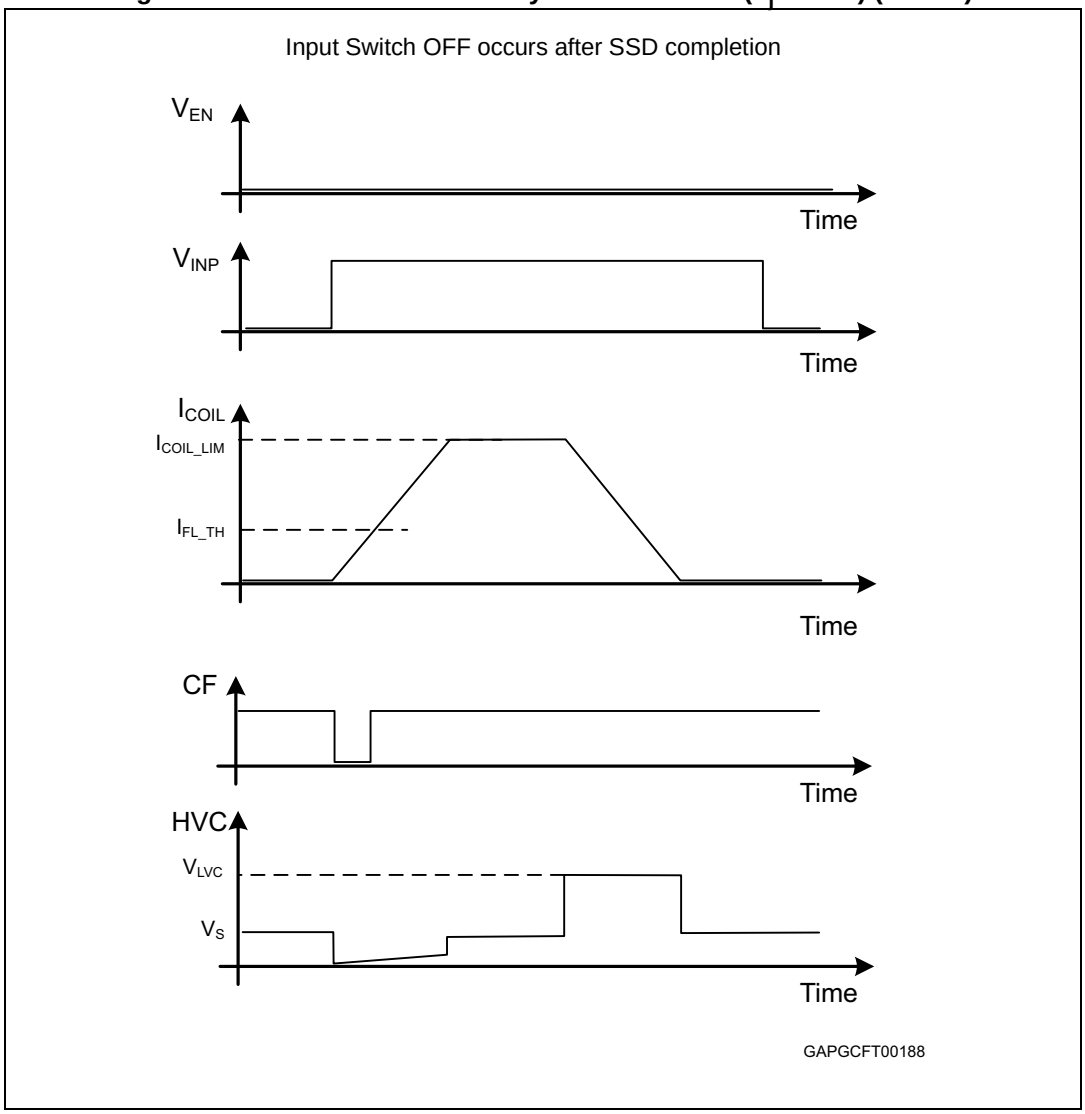


Figure 9. Current limit followed by TSD activation (T_j = TSD) (case 2)

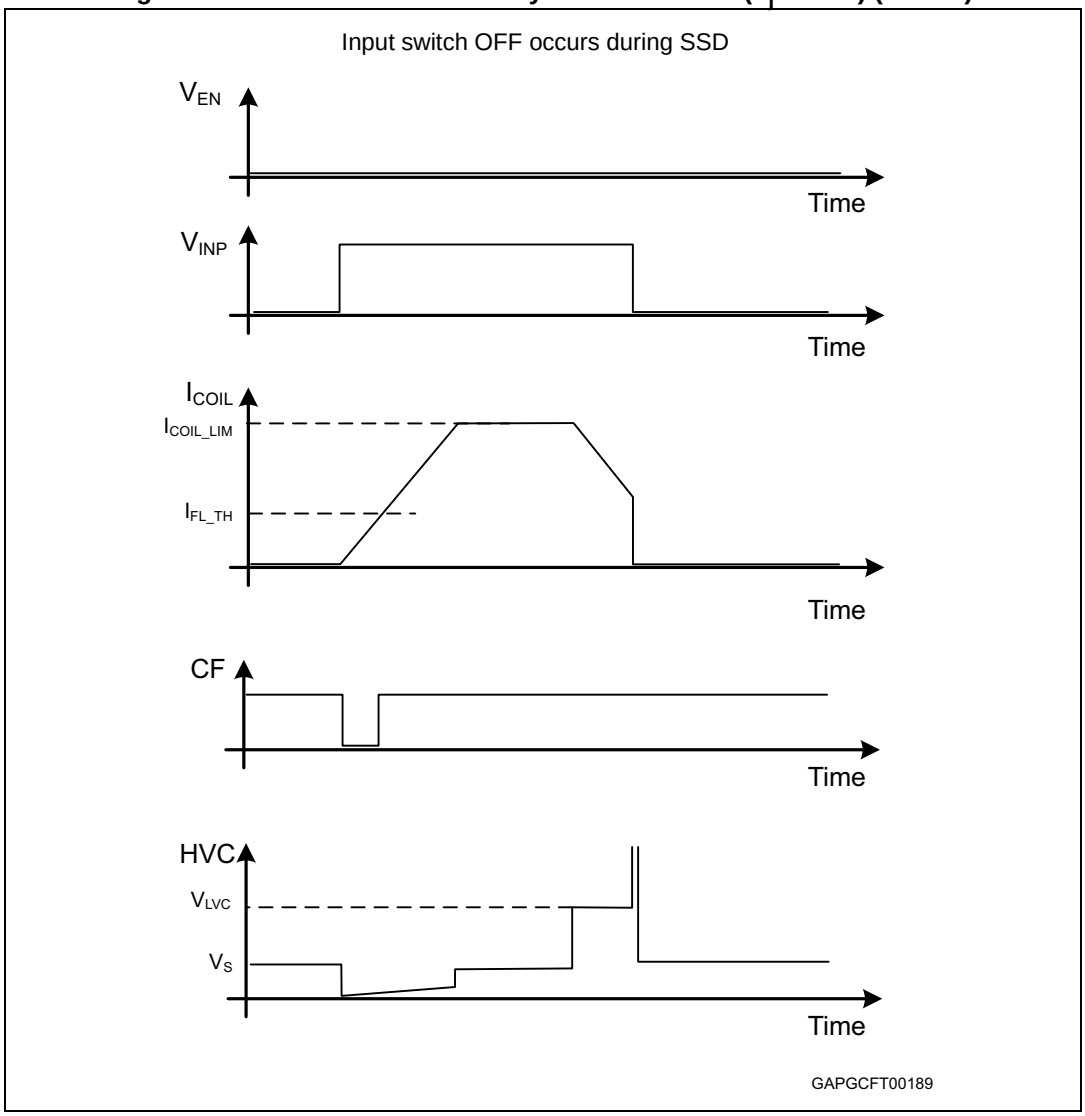


Figure 10. Thermal cycling behavior

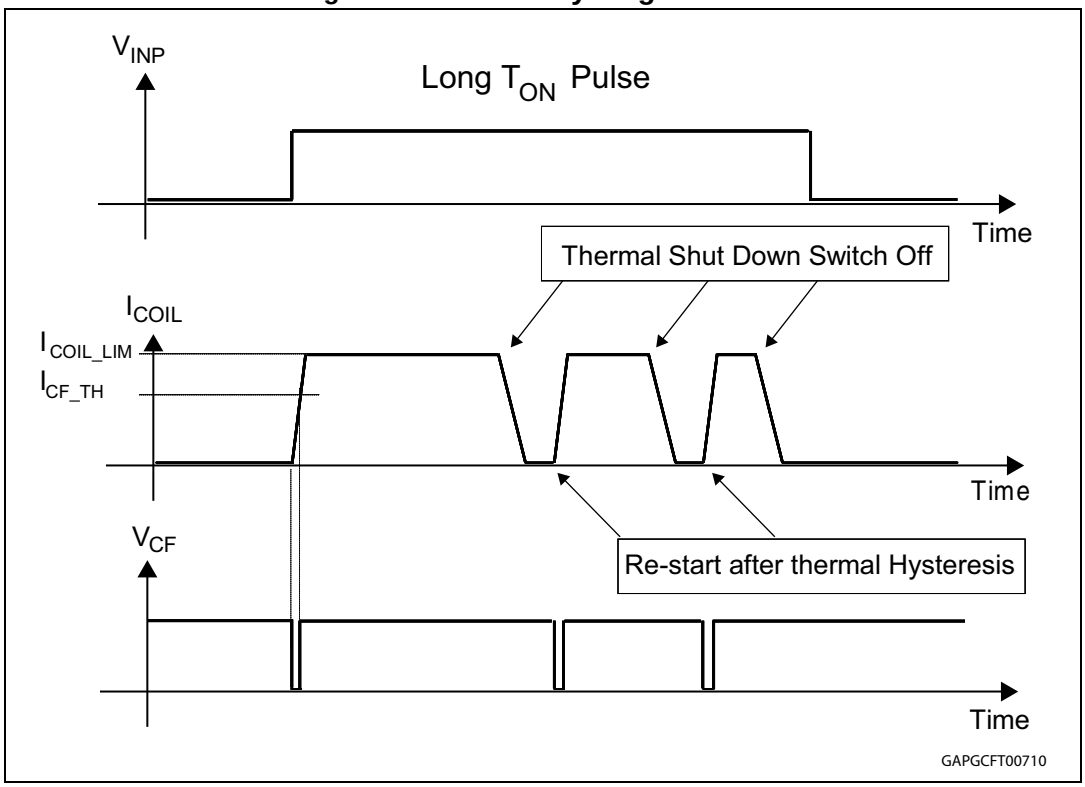


Figure 11. Switch on attempt at $T_j > T_{SSD}$

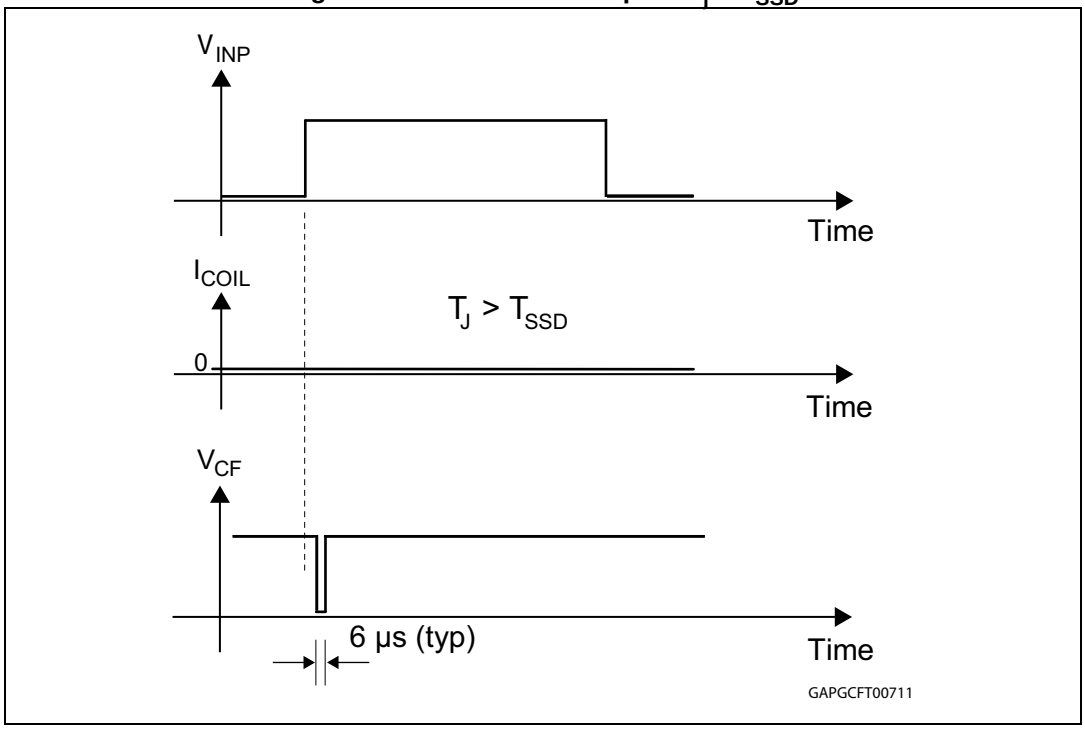


Figure 12. Soft switch off caused by EN pin pulled high

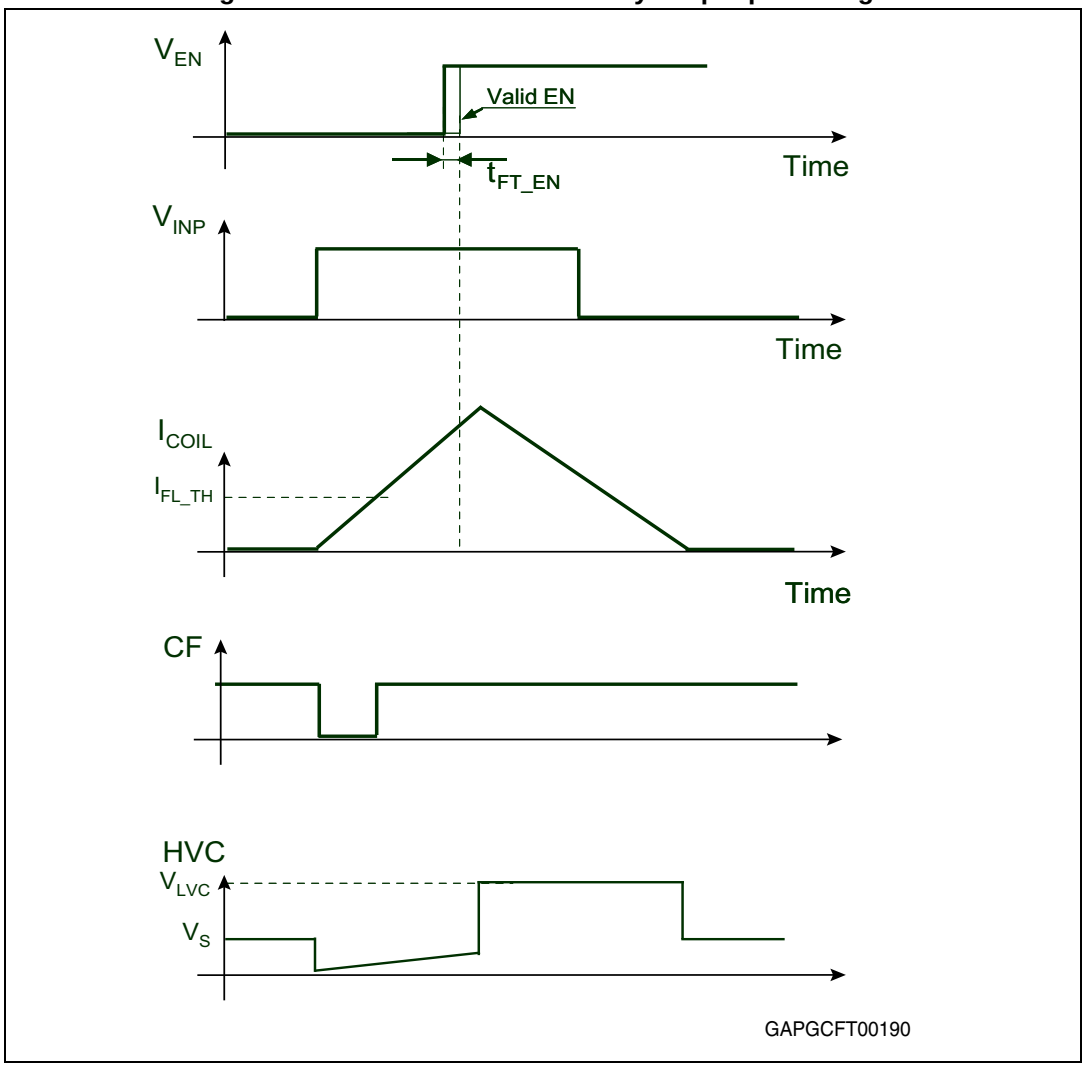


Figure 13. Coil current discharge completion after releasing of EN pin

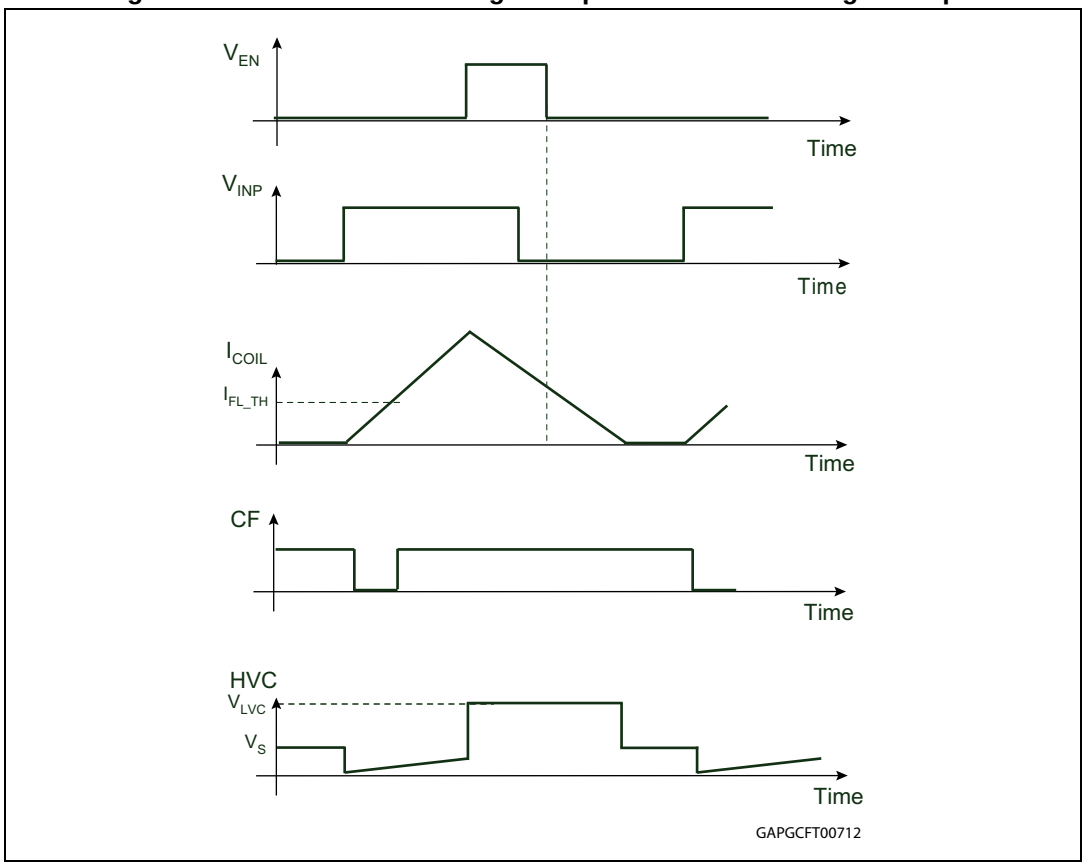


Figure 14. Device behaviour when EN pin becomes high before low to high transition of Input command

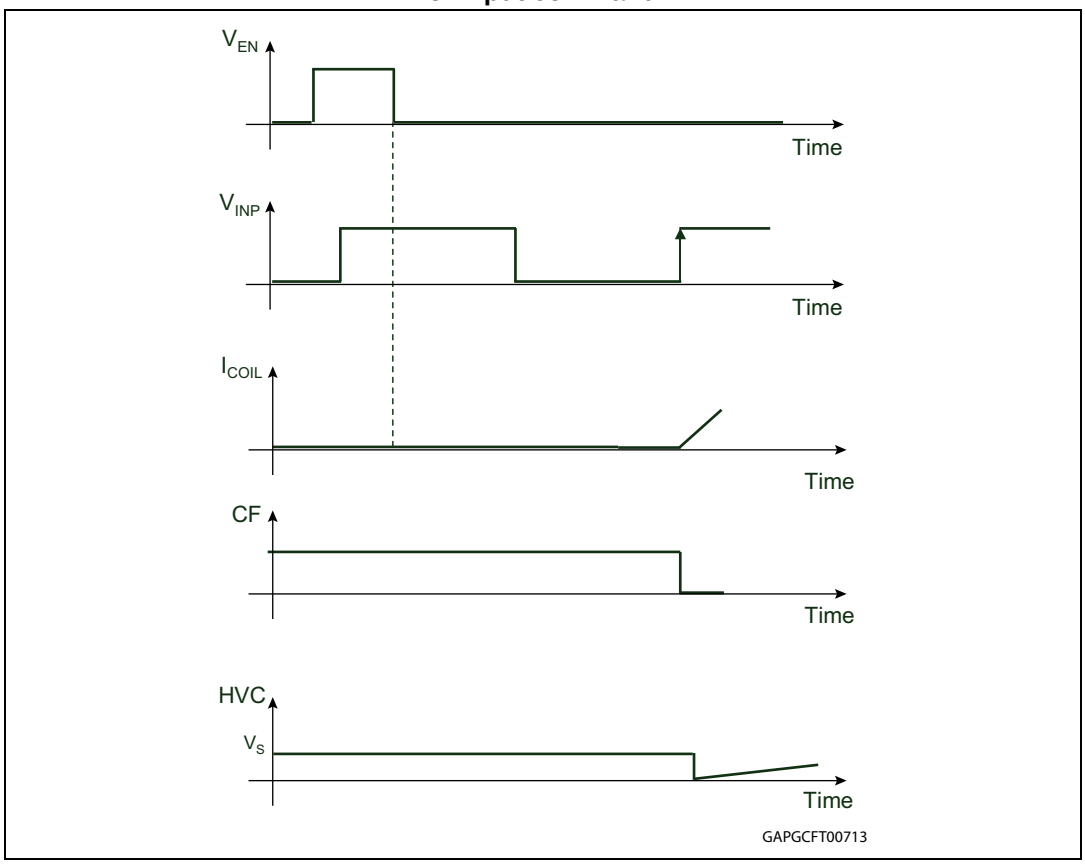


Figure 15. Device behaviour when EN pin is pulled up and down while Input command is still high

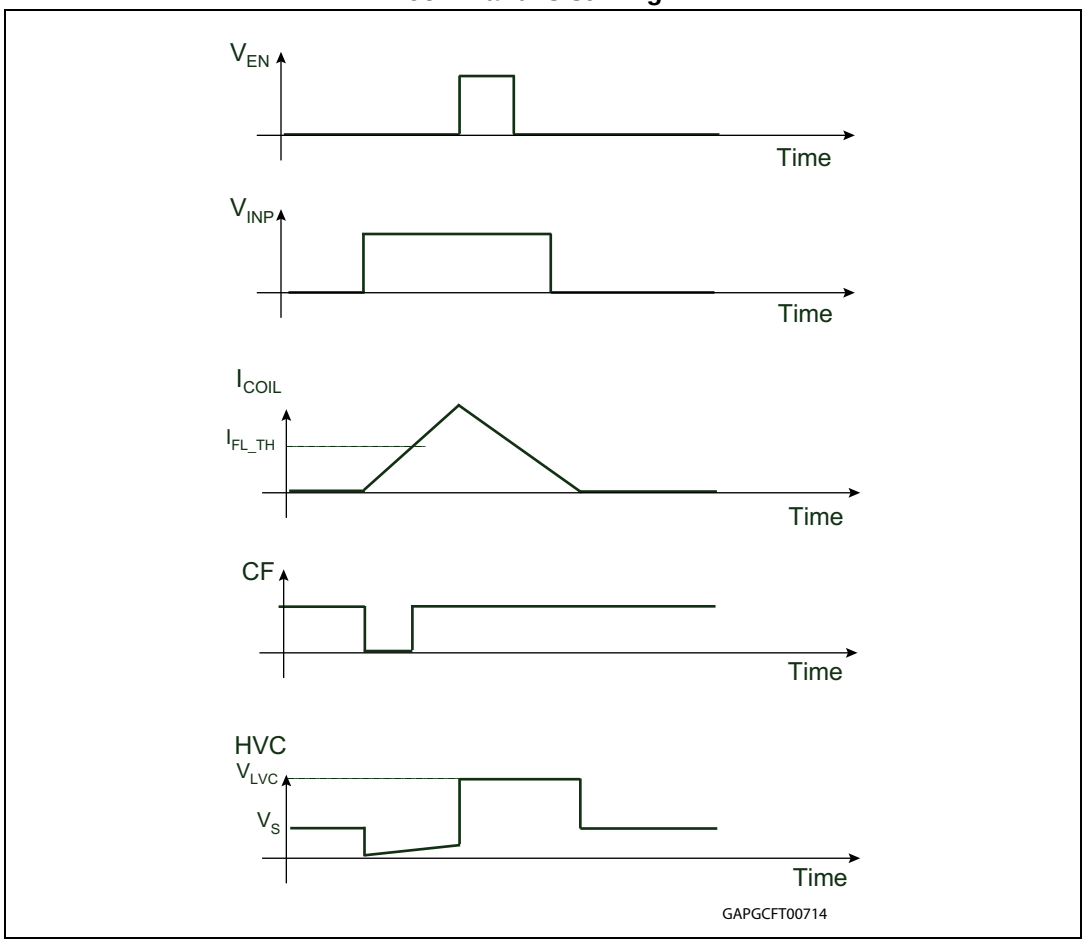


Figure 16. Device behavior in case of Input over voltage

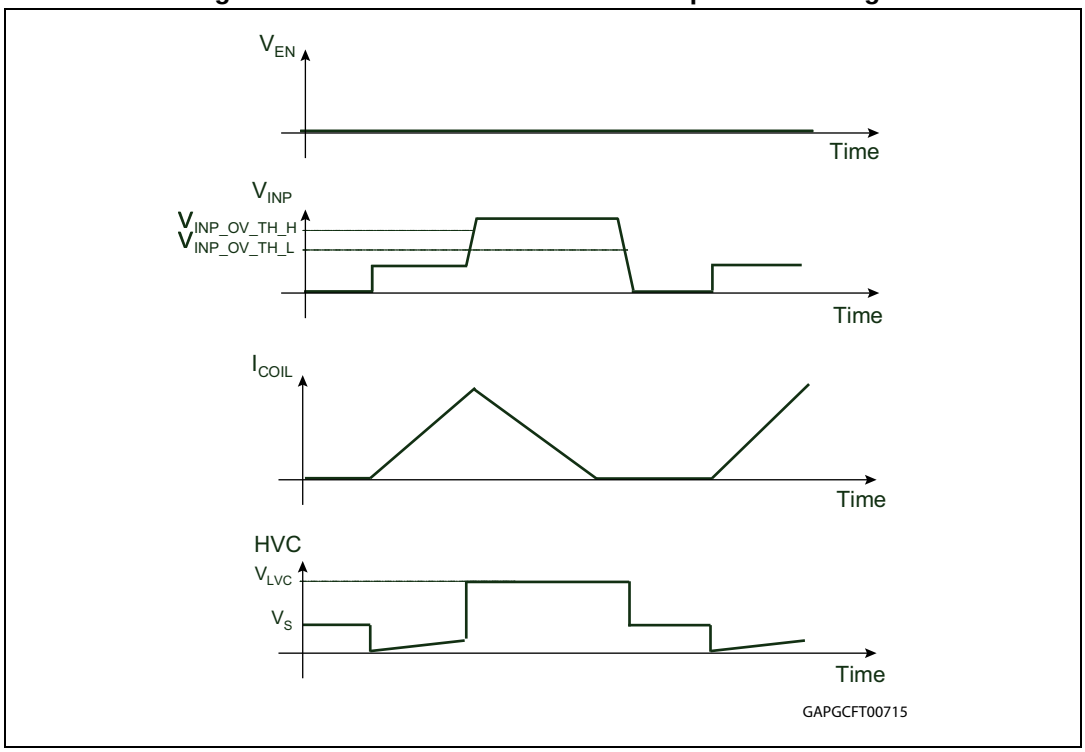


Figure 17. Device behavior in case of battery over voltage

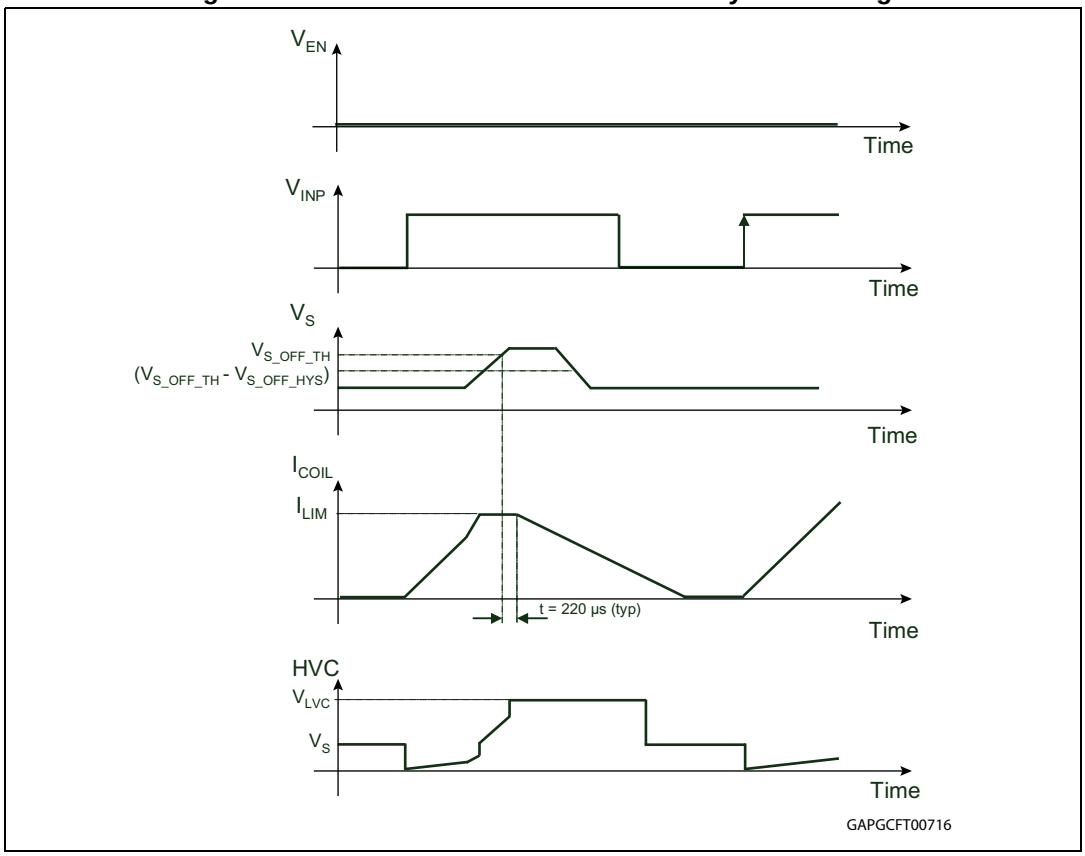


Figure 18. Current flag threshold vs temperature for I_{FLAG} = 6.5 A

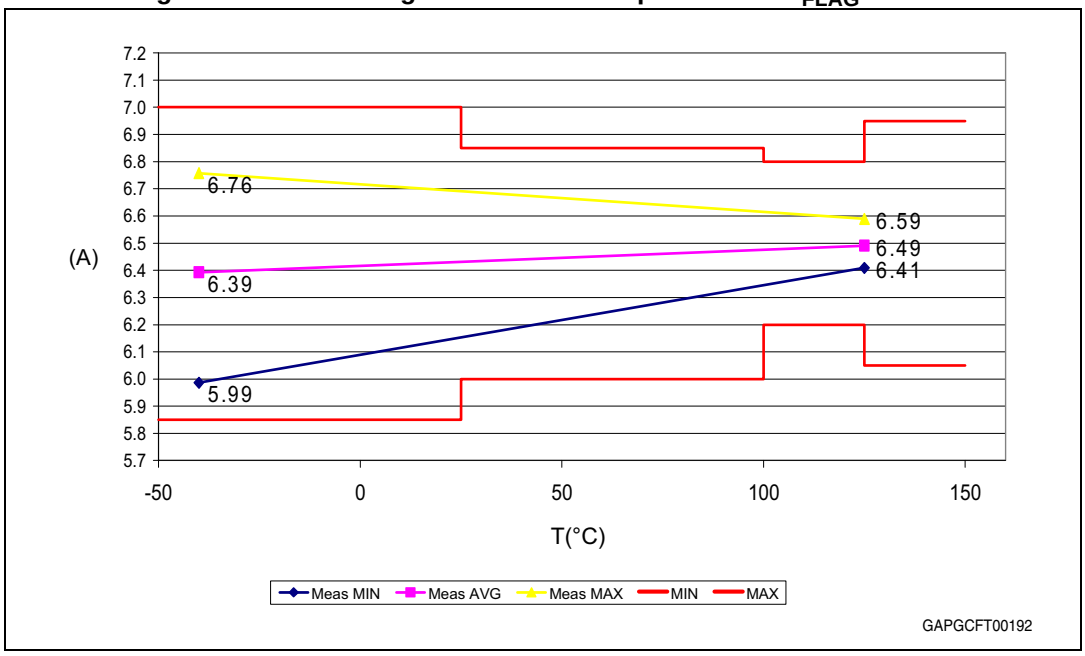
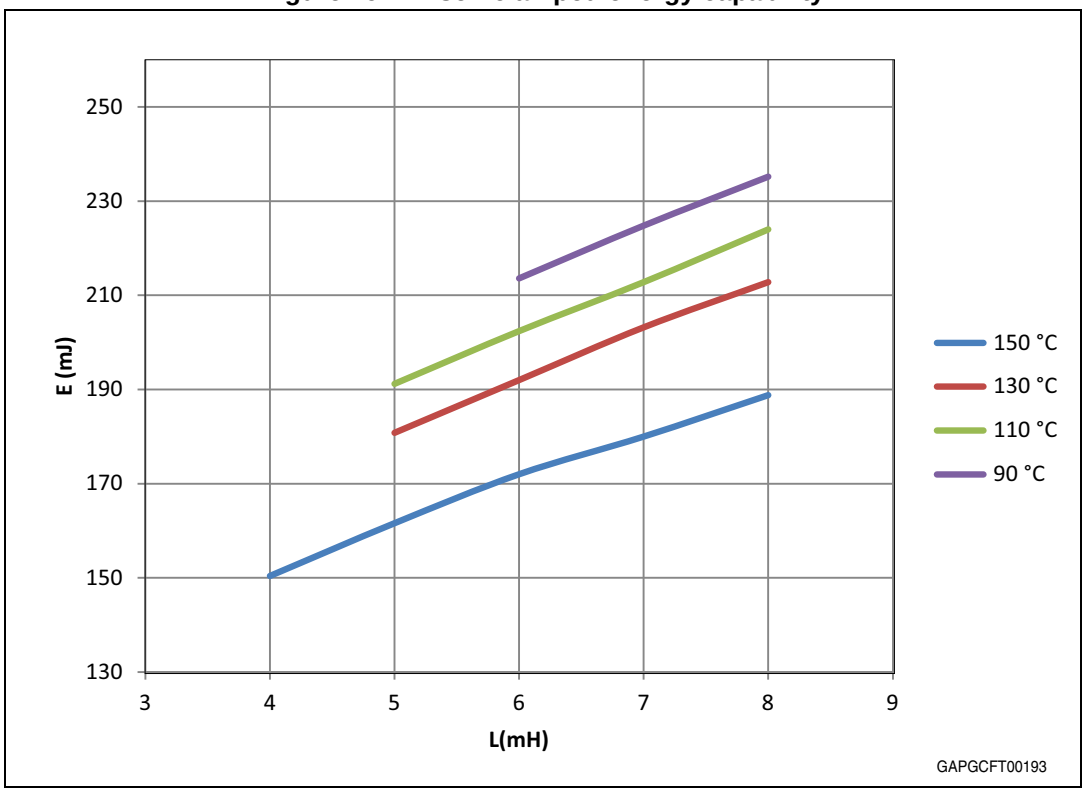


Figure 19. HV self clamped energy capability



4 Electrical transient requirements

4.1 General setup

All ISO pulses are performed according to the following schematics (see *Figure 20* and *Figure 21*).

All ground pins (PGND1, GND and PGND2) are connected together as short as possible on the test board. The other pins (INP, EN, CF) are left open.

The load resistor is a nominal resistor 2 Ω. For breakdown level, for ISO1 and 2a 10 pulses are applied, and for ISO3a and 3b, test is applied during 1 minute.

Figure 20. General ISO Pulse schematic

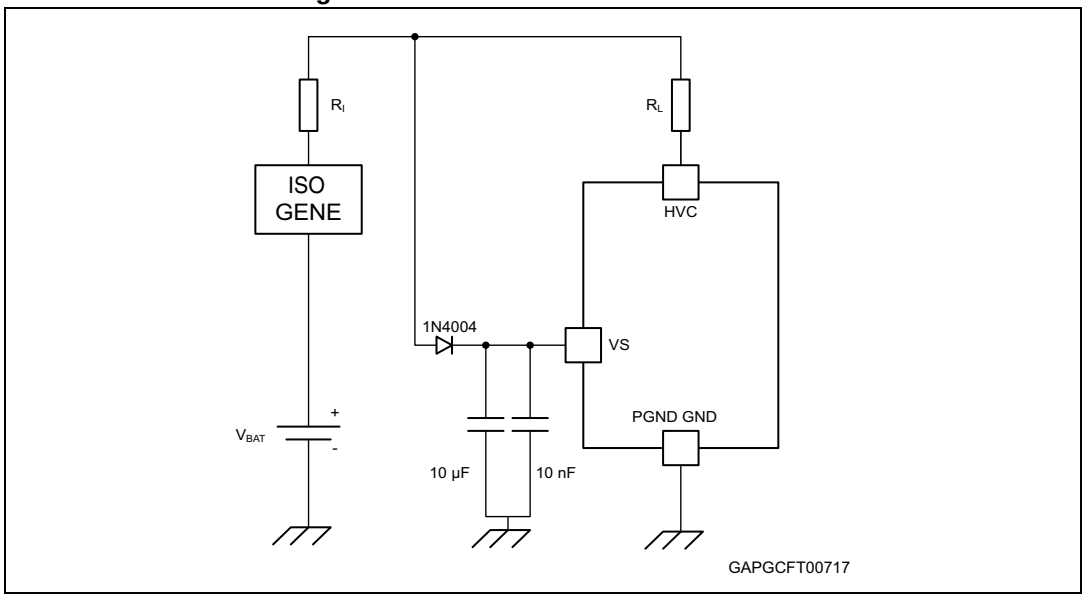


Figure 21. ISO Pulse schematic for pulse type 5b

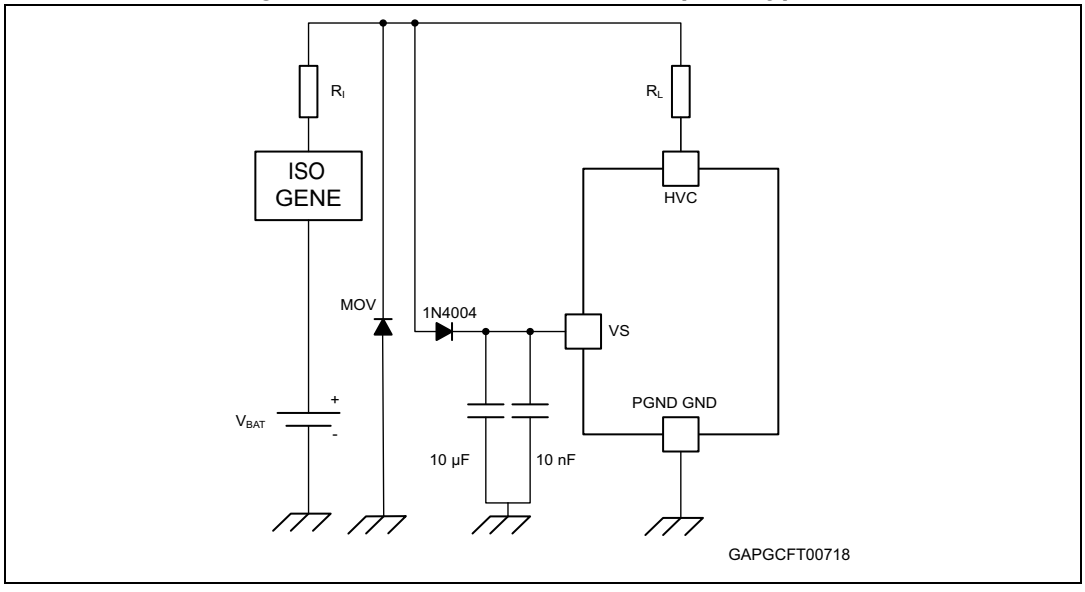


Table 8. Electrical transient requirements (part 1/3)

ISO 7637-2 2004 (E) Test Pulse	Test level		Number of pulse or test times	Burst cycle / pulse repetition time		Delay and impedance
	III	IV				
1	-75	-100	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37	+50	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1 h	90 ms	100 ms	50 µs, 2 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(1)	65	8 V	1 pulse			100 ms, 0.01 Ω

1. External load dump clamp, 40 V max, refereed to ground.

Table 9. Electrical transient requirements (part 2/3)

ISO 7637-2 2004 (E) Test Pulse	Test level	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

1. External load dump clamp, 40V max, refereed to ground.

Table 10. Electrical transient requirements (part 3/3)

Class	Content
C	All function of the device is performed as designed after exposure to disturbance
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

5 PCB layout suggestions and PGND disconnection

Device is provided with two power gnd leads perfectly symmetrical. Therefore, the current flowing trough each lead is exactly half of the one flowing trough coil and IGBT power stage collector. PCB power GNDs tracks must be as much symmetrical as possible respect to the Power GND node, in order to always maintain $I_{PGND1} = I_{PGND2}$ (see *Figure 4*).

A difference voltage V, between P_{GND1} an P_{GND2} causes a misalignment between I_{COIL_LIM} and I_{CF_TH}.

In case of only P_{GND2} disconnection the device is still operative, but its coil current is limited till a maximum value of ½ I_{COIL_LIM}. Current Flag signal operates, but its threshold value is also reduced at ½ I_{CF_TH}.

If, instead, only P_{GND1} is disconnected from the power GND, the coil current is controlled only by the width of input command signal (no limitation). Furthermore, the C.F. signal is kept in the low state for all duration of Input command signal.

6 Package and PCB thermal data

6.1 OctaPAK thermal data

Figure 22. OctaPAK on two-layers PCB

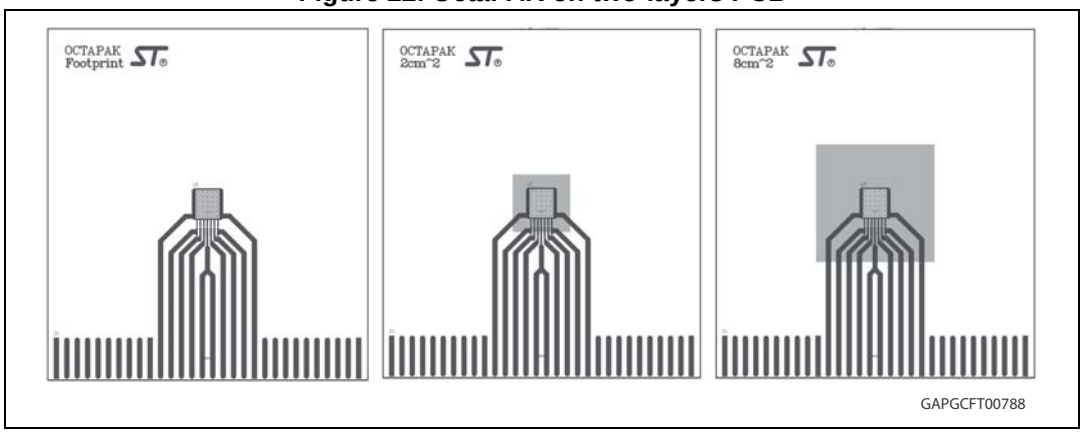


Figure 23. OctaPAK on four-layers PCB

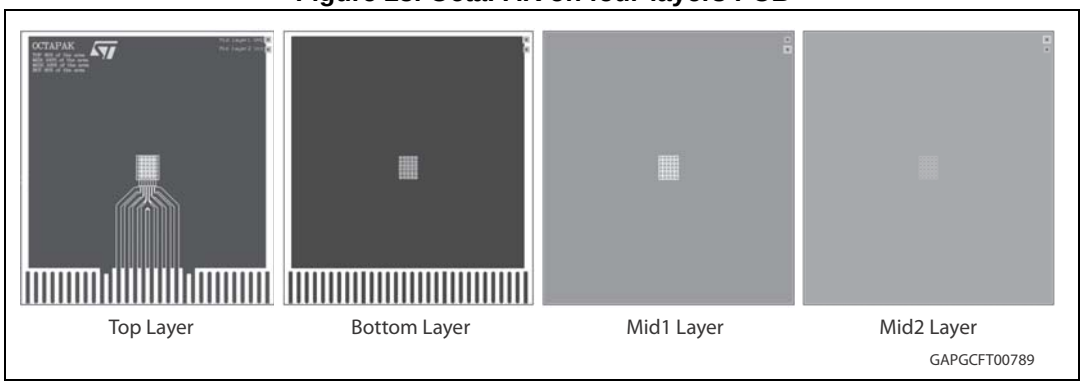


Table 11. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	78 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension	6.4 mm x 7mm

Figure 24. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

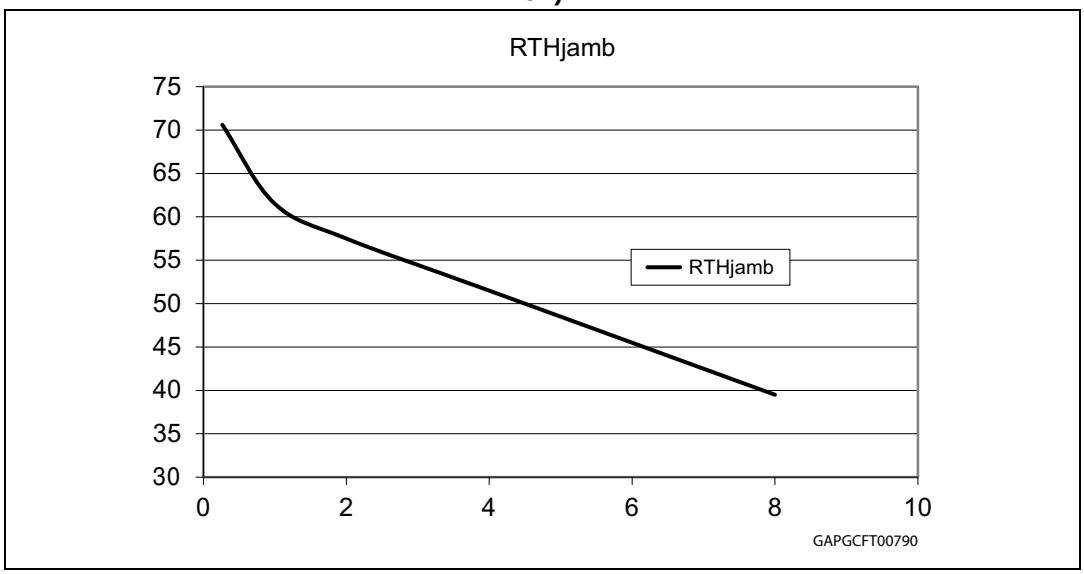
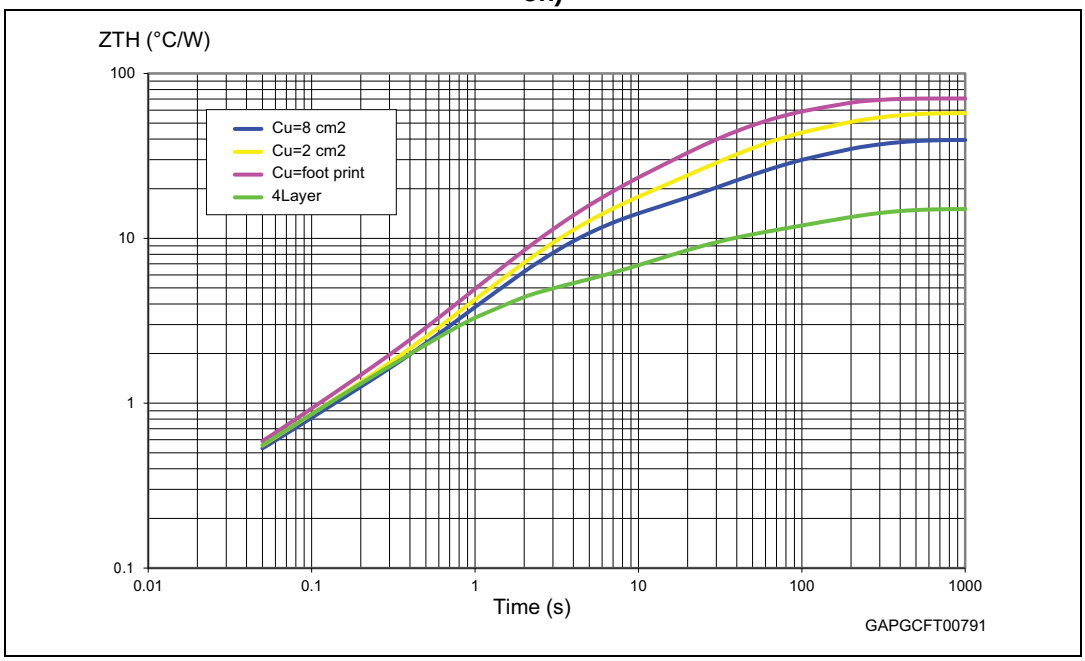


Figure 25. OctaPAK thermal impedance junction ambient single pulse (one channel on)

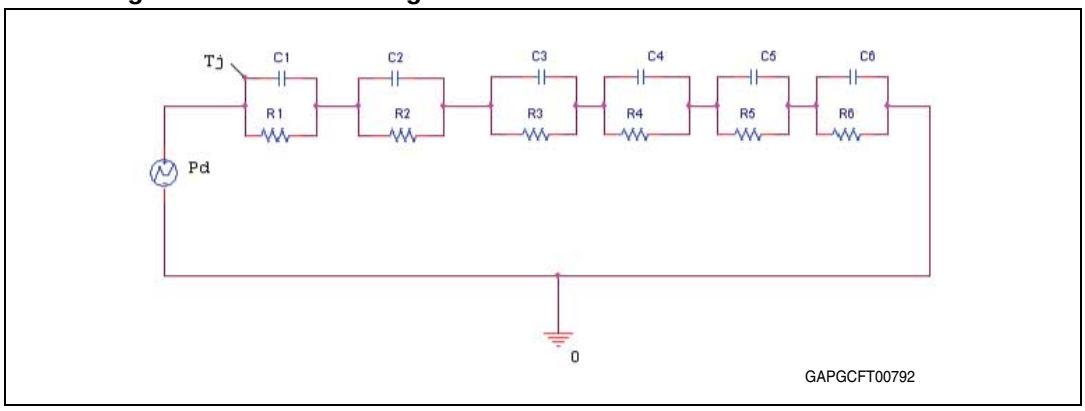


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Figure 26. Thermal fitting model of a double-channel HSD in OctaPAK



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 12. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	0.01	0.01	0.01	0.01
R2 (°C/W)	0.15	0.15	0.15	0.15
R3 (°C/W)	0.4	0.4	0.4	0.4
R4 (°C/W)	10	10	10	3.5
R5 (°C/W)	28	22	12	5
R6 (°C/W)	32	25	17	6
C1 (W.s/°C)	0.005	0.005	0.005	0.005
C2 (W.s/°C)	0.05	0.05	0.05	0.05
C3 (W.s/°C)	0.2	0.2	0.2	0.2
C4 (W.s/°C)	0.3	0.3	0.3	0.25
C5 (W.s/°C)	0.8	1.4	3	3
C6 (W.s/°C)	3	6	9	25

7 Package informations

7.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.2 OctaPAK package information

Figure 27. OctaPAK package dimensions

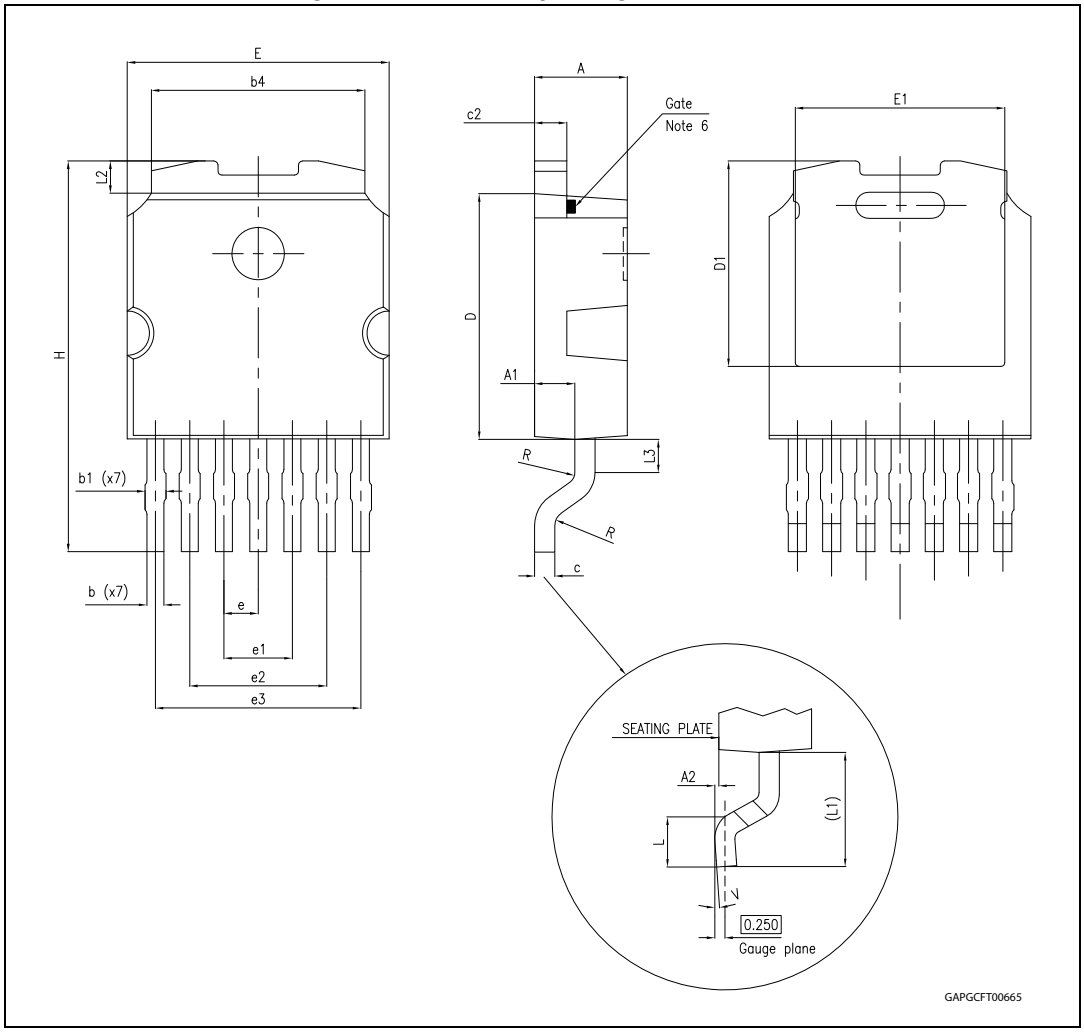


Table 13. OctaPAK mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.00	1.10
A2	0.03	0.10	0.23
b	0.45	0.52	0.60
b1			0.70
b4	5.20	5.30	5.40
c	0.45	0.50	0.60
c2	0.75	0.80	0.90
D	6.00	6.10	6.20
D1		5.15	
E	6.40	6.50	6.60
E1		5.30	
e		0.85	
e1	1.60	1.70	1.80
e2	3.30	3.40	3.50
e3	5.00	5.10	5.20
H	9.35	9.70	10.10
L	1.00		—
(L1)		2.80	
L2		0.80	
L3		0.85	
R	0.40		0.65
V2	0°		8°

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
28-Mar-2013	1	Initial release
16-Sep-2013	2	Updated disclaimer

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